

Compiler and Tool Support for Enhancing Programmer Productivity: Loop Fusion and Hardware-in-the-Loop Simulation

**By
Dr. Gerald Baumgartner**

Date: March 14th, Friday.
Time: 1:00 PM
Venue: 256 Coates Hall

Abstract

The goal of my research is to build novel tools for enhancing the productivity of programmers, ranging from language design to compiler optimizations to software testing tools. In this talk I will focus on two recent projects on loop fusion optimization and on a simulation- based embedded systems testing tool.

In the context of the Tensor Contraction Engine, we have previously developed a cost-model driven loop fusion optimization algorithm for minimizing memory requirements and disk I/O. This algorithm relies on a high-level representation and the simple mathematical structure of tensor contraction code. I will show how this algorithm can be extended to hand-written code so it could be used in a traditional compiler.

Testing of embedded systems code is complicated by the interactions between an embedded processor and the electrical and mechanical devices controlled by that processor. The automotive and aircraft industries employ hardware-in-the-loop simulations that rely on dedicated simulation computers and special purpose hardware. We have developed a low-cost hardware-in-the-loop simulation environment based on a virtual embedded processor. I will describe the architecture of this environment and show how it, combined with an automaton-based testing tool, can be used for building a test harness for embedded code.