

Computer Science Ph.D. General Examination—Spring 1999
Computer Architectures

Answer **three** of the following four questions.

1. Answer the following questions on the binary n -cube (hypercube) network of processors.
 - a. What is the node degree?
 - b. What is the network diameter?
 - c. What is the bisection width?
 - d. Consider a global reduction operation in which every processor starts with one value and needs to know the sum of the values stored at all the processors. Briefly describe an algorithm to perform the global reduction operation in n steps.

2. Consider a cache with 64 Kbytes and a main memory with 32 Mbytes. A cache block has 32 bytes corresponding to eight 32-bit words. (Assume that the memory is word addressable.)
 - a. Show the direct mapping address format by giving the tag field, the block number, the word number, and the number of bits for each of these three fields.
 - b. Show the full associative mapping address format by giving the tag field, the word number, and the number of bits for each of these two fields.
 - c. Show the 2-way set associative mapping address format by giving the tag field, the set number, the word number, and the number of bits for each of these three fields.
 - d. The access time of the cache, main memory, and magnetic disk is $t_1 = 10$ ns, $t_2 = 100$ ns, and $t_3 = 10$ ms, respectively. What is the effective access time assuming the cache hit ratio $h_1 = 0.9$ and the hit ratio $h_2 = 0.99$ in the main memory?

3.
 - a. What is the superpipelined architecture?
 - b. What is the superscalar architecture?
 - c. What is the VLIW (very long instruction word) architecture?
 - d. Derive the speedup formula $S(m,n)$ for a superpipelined superscalar computer of degree (m, n) with k stages in the pipeline.

4. A virtual memory system has an address space of 8K words, a memory space of 4K words, and page and block sizes of 1K words. The following page reference changes occur during a given time interval.

4 2 0 1 2 6 1 4 0 1

 - a. Determine the four pages that are resident after each page reference change if the page-replacement algorithm used is (i) FIFO (first in first out); (ii) LRU (least recently used).
 - b. What is the hit ratio in the main memory if the page-replacement algorithm used is (i) FIFO; (ii) LRU?